

**Title: Ternary Digital System: Concepts and Applications**

**Authors: A P Dhande, V T Ingole, V R Ghiye**

**Published by SM Online Publishers LLC**

**Copyright © 2014 SM Online Publishers LLC**

**ISBN: 978-0-9962745-0-0**

All book chapters are Open Access distributed under the Creative Commons Attribution 3.0 license, which allows users to download, copy and build upon published articles even for commercial purposes, as long as the author and publisher are properly credited, which ensures maximum dissemination and a wider impact of the publication. Upon publication of the eBook, authors have the right to republish it, in whole or part, in any publication of which they are the author, and to make other personal use of the work, identifying the original source.

Statements and opinions expressed in the book are these of the individual contributors and not necessarily those of the editors or publisher. No responsibility is accepted for the accuracy of information contained in the published chapters. The publisher assumes no responsibility for any damage or injury to persons or property arising out of the use of any materials, instructions, methods or ideas contained in the book.

First published October, 2014

Online Edition available at [www.smgebooks.com](http://www.smgebooks.com)

For reprints, please contact us at [ebooks@esciencemedicine.com](mailto:ebooks@esciencemedicine.com)

# Ternary Arithmetic Operations

## INTRODUCTION

We all are familiar with the arithmetic operations like addition, subtraction, multiplication and division of decimal number. Similar operations can be performed on ternary numbers. The rules for ternary addition, subtraction, multiplication and division are different but these are closely related to binary arithmetic operations.

## TERNARY ARITHMETIC

### Ternary Addition

Rules for ternary addition are given in table 2.1.

**Table 2.1:** Ternary addition rules.

Augend	Addend	Sum	Carry	Result
0	0	0	0	00
0	1	1	0	01
0	2	2	0	02
1	1	2	0	02
1	2	0	1	10
2	2	1	1	11

**Explanation:** Let augend be equal to 0, addend be equal to 0 it gives  $\text{Sum} = 0 + 0 = 0$  and no carry generated so carry = 0 as shown in table 2.1. If when augend be equal to 1, addend be equal to 2 we get  $1 + 2 = 3$ . i.e. representation for 3 in ternary is 01 that implies sum = 0 and carry = 1. Similarly when augend be equal to 2, addend be equal to 2 we get  $2 + 2 = 4$ . i.e. representation for 4 in ternary is 11 that implies sum = 1 and carry = 1.

Consider an example

Let Augend A = 64 and Addend B = 48

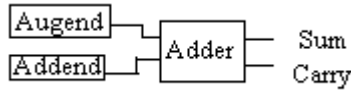
So  $A + B = 112$

Ternary representation for 64 and 48 are 02101 and 01210 respectively.

According to rules given in table 2.1. we can perform addition as:

$$\begin{array}{r}
 A = 64 = 02101 \\
 + B = 48 = 01210 \\
 \hline
 \text{Sum} = 112 = 11011
 \end{array}$$

General block diagram for ternary adder is shown below and detail design and logic gate level implementation of circuit for half and full is described in chapter 5.



Block diagram for ternary Adder.

## Ternary Subtraction

Rules for ternary subtraction are given in table 2.2.

**Table 2.2:** Ternary subtraction rules

Minuend	Subtrahend	Difference	Borrow	Result
0	0	0	0	00
0	1	2	1	
0	2	1	1	
1	1	0	0	
1	2	2	2	
2	2	0	0	

**Explanation:** Let Minuend be equal to 0, Subtrahend be equal to 0 it gives Difference =  $0 - 0 = 0$  and no Borrow generated so Borrow = 0 as shown in table 2.2. If when Minuend be equal to 1, Subtrahend be equal to 2 we get  $1 - 2 = -1$ . i.e. representation for 3 in ternary is 01 that implies Difference = 0 and borrow = 1. Similarly when Minuend be equal to 2, Subtrahend be equal to 2 we get  $2 - 2 = 0$ . i.e. representation for 0 in ternary is 00 that implies Difference = 0 and borrow = 0.

Consider an example

Let Minuend  $A = (64)_{10}$  and Subtrahend  $B = (48)_{10}$

So  $A - B = (16)_{10}$

Ternary representation for 64 and 48 are  $(02101)_3$  and  $(01210)_3$  respectively.

According to rules given in table 2.2. we can perform subtraction as:

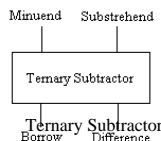
Let  $A = 02101 = 64$  and  $B = 01210 = 48$ ,  $-48$  can be represented as 21012, it is 1's complement of 48. by adding 1 to 1's complement of 48 we get 3's complement of 48 i.e.  $21012 + 1 = 21020$

(Details about 1's and 3's complement is explained in chapter 1.)

So  $A - B = 02101$

$$\begin{array}{r} 02101 \\ + 21020 \\ \hline 100121 \end{array}$$

Discarding left most digit, the answer is  $(00121)_3$  which is equivalent to  $(16)_{10}$ . Block for ternary subtractor is shown in figure 2.2 and details are explained in chapter 5.



# Ternary Multiplication

**Table 2.3:** Rules for ternary multiplications.

Multiplicand	Multiplier	Product	Carry	Result
0	0	0	0	00
0	1	0	0	00
0	2	0	0	00
1	1	1	0	01
1	2	2	0	02
2	2	1	1	11

**Explanation:** Let Multiplicand be equal to 0, Multiplier be equal to 0 it gives product = 0 and carry = 0 as shown in table 2.3. If when Multiplicand be equal to 1, Multiplier be equal to 2 we get  $1 \times 2 = 2$ . i.e. representation for 2 in ternary is 02 that implies product = 2 and carry = 0. Similarly when Multiplicand be equal to 2, Multiplier be equal to 2 we get  $2 \times 2 = 4$ . i.e. representation for 4 in ternary is 11 that implies sum = 1 and carry = 1.

**Example:** Let Multiplicand A =  $(15)_{10}$  and B =  $(11)_{10}$

So, 15

$$\begin{array}{r} \text{X } 11 \\ \hline (165)_{10} \end{array}$$

Now  $(120)_3$  is ternary representation for  $(15)_{10}$  and  $(102)_3$  is representation for  $(11)_{10}$

i.e.  $120 (15)_{10}$

$$\begin{array}{r} \text{X } 102 (11)_{10} \\ \hline 1010 \\ + 000x \\ + 120xx \\ \hline 20010 (165)_{10} \end{array}$$

By applying the rules in table 2.3.3 the result is 20010 which is ternary representation for 165.

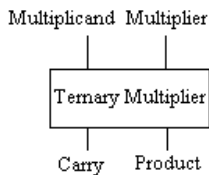


Figure above is for ternary multiplier and detail about design, gate level implementation and circuit is explained in chapter 5.

# Ternary Division

It is performed in the same way as binary division. Rules are as below.

- 1) If Dividend is greater than or equal to divisor, put value to quotient and subtract divisor from dividend.
- 2) Shift the divisor one place right and perform step 1 up to dividend is smaller than the divisor.
- 3) If remainder is non zero, repeat step 1 by putting corresponding values to remainder.
- 4) Repeat until dividend is less than the divisor and quotient is correct. The dividend is the remainder.

**Example 1:** Let  $A = (30)_{10} = 1010$  is ternary representation and  $B = (10)_{10} = 101$  is representation for  $(10)_{10}$ . Therefore  $A \div B = (30)_{10} \div (10)_{10} = 1010 \div 101 = 10$  which is ternary representation for  $(3)_{10}$

$$\begin{array}{r}
 10 \\
 10 \ 1 \sqrt{1010} \\
 \underline{-101} \\
 000 \\
 \underline{-000} \\
 000
 \end{array}$$

**Example 2:** Let  $A = (15)_{10}$  and  $B = (3)_{10}$  So  $A \div B = (5)_{10}$   
 i.e.  $(120)_3 \div (10)_3 = (12)_3$

$$\begin{array}{r}
 12 \\
 11 \ \sqrt{120} \\
 \underline{-10} \\
 020 \\
 \underline{-20} \\
 00
 \end{array}$$

## SUMMARY

Various number systems that are used in digital circuits, microprocessor, computers etc have been presented. The rules of ternary arithmetic operations like addition, subtraction, multiplication, division are given.

The knowledge of this number system is essential for effective understanding of various ternary circuits.

## References

1. Shimabukuro K, Zukeran C. Reconfigurable current-mode multiple-valued residue arithmetic circuits. Proc. 28<sup>th</sup> Int Symp. Multiple-Valued Logic. 1998; 282-287.
2. Wei S, Shimizu K. Residue arithmetic multiplier based on the radix-4 signed-digit multiple-valued arithmetic circuits, 12<sup>th</sup> Int Conf. on VLSI Design. 1999; 212-217.
3. Hanyu T, Kameyama M. A 200 MHz pipelined multiplier using 1.5 V-supply multiple valued MOS current-mode circuits with dual-rail source-coupled logic. IEEE Journal of Solid-State Circuits. 1995; **30**: 1239-1245.
4. Gonzalez F, Mazumder P. Multiple-valued signed digit adder using negative differential resistance devices. IEEE Trans. on Computers. 1998; **47**: 947 - 959.
5. Radanovic M, Szyrzycki. Current-mode CMOS adders using multiple-valued logic. Canadian Conference on Electrical and Computer Engineering. 1996; 190-193.
6. Ishizuka O, Handoko D. VLSI design of a quaternary multiplier with direct generation of partial products. Proc 27<sup>th</sup> Int Symp. Multiple-Valued Logic. 1997; 169-174.
7. Saed A, Ahmadi M, Jullien GA. Arithmetic with signed analog digits, Proc 14<sup>th</sup> IEEE Symposium on Computer Arithmetic. 1999; 134-141.
8. Ohki Y, Aoki T, Higuchi T. Redundant complex number systems, Proc 25<sup>th</sup> Int Symp. Multiple-Valued Logic. 1995; 14-19.